REMARKS

This Response is submitted with respect to the Office Action dated May 31, 2006.

I. THE EXAMINER'S CLAIM REJECTIONS UNDER 35 U.S.C. § 103 ARE UNSUPPORTABLE AND SHOULD BE WITHDRAWN.

At paragraph 6 of the present Office Action, Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,263,303 to Yu, *et al.* (*Yu*) in view of the article "Direct Access Storage Device (DASD) modeling and validation" by Lim *et al.* (*Lim*). Applicants respectfully traverse each of these rejections in light of the arguments contained below.

(A) The proposed combination does not teach or suggest the recited elements of Applicant's claims.

With respect to exemplary Claim 1, to dependent claims 2-19, and to similar claim 20, Applicant respectfully submits that the Examiner's proposed combination of *Yu* and *Lim* does not render obvious Applicant's invention, because the proposed combination does not teach or suggest the claimed features of Applicant's invention for which it is cited.

At paragraph 7, the Examiner alleges that *Yu* teaches "providing a testing program for interacting with said control program module and said software representation of said plurality of hardware components". Applicant respectfully submits that the combination of *Yu* and *Lim* does not teach or suggest "instructions on the computer readable medium for providing a testing program for interacting with said control program module and said software representation of said plurality of hardware components", as recited in Applicant's exemplary Claim 1.

The Examiner has, also in paragraph 7, identified core **18** as representing the recited control program module and module **16** as representing the recited software representation of the plurality of hardware components. It logically follows that, in order to sustain a rejection consistent with the Examiner's mapping, the feature identified by the Examiner as a "testing program for interacting with said control program module and said software representation" must

interact with core **18** and module **16**. Otherwise, the recited "interacting with said control program module and said software representation of said plurality of hardware components" is neither taught nor suggested by the combination of *Yu* and *Lim*.

Unfortunately, no such interaction is taught or suggested by the combination of *Yu* and *Lim*. The Examiner cites **Figure 5D** as teaching the recited functionality. Figure 5D is explained at Column 8, line 34- Column 9, line 25, which disclose:

> Referring now to **FIG. 5D**, the main simulation process **120** can be described. This process primarily manages the delivery of triggers stored on the event queue shown in **FIG. 6**, so as to move the simulation process forward in a pseudo cycle-driven manner. In step **122**, the process begins at the first entry in the event queue. Initialization of the simulation process is performed by installing, into the first or subsequent entries in the event, channel or event function triggers simulating the initialization of the simulated system. Accordingly, the first entry in the event queue will typically include one or more triggers to channels or event functions to initialize the simulation.
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> In step **124**, the main simulation process triggers all channels and event functions listed in the current (first) entry of the event queue, using the values and state/arguments that are stored in the list of triggers in the current entry. Then in step **126**, if there is an adapter for a concurrent simulation, the channels connected to the adapter are triggered with any input signals being produced by the adapter.
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> The triggers produced in steps **124** and **126** will generate a chain reaction of calculations and triggers that will continue through the simulated system. Specifically, channels triggered in step **124** or **126** will trigger transition objects, some of which will transition event functions. Some of these event functions will trigger channels, which may then trigger additional transition objects and additional event functions. Also, event functions triggered in step **124** will similarly trigger transition objects and event functions. As this chain reaction continues, future triggers for channels and/or event functions will be stored on the event queue through the operation of event functions as described above with reference to **FIG. 5C**.
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> In step **128**, the main simulation process awaits the end of this chain reaction of triggers, until the last triggered process returns. Ultimately, under normal circumstances, the chain reaction of triggers initiated in steps **124** and **126** will terminate, at which time the event queue entries after the current entry will typically contain lists of stored triggers for channels and event functions. These stored triggers identify actions that will be completed in future times in accordance with the simulation models used in the original module definitions used in the simulation.

> After ending the wait in step **128**, in step **130** the values found on the channels, representing the results of the first cycle of simulation, are applied to the adapter(s) used in the simulation, so as to stimulate the external simulations connected via the adapter(s). Then, in step **132**, the main simulation process moves to the next entry in the event queue and processing returns to step **124**, in which the various stored triggers in the current (second) entry of the event queue are delivered to the identified channels and event functions, and to step **126** where triggers corresponding to inputs from adapter(s) are delivered to channels, thus again triggering a chain reaction of triggers simulating the activity of a second cycle of simulation.
>
> The loop including steps **124, 126, 128, 130** and **132** is then repeated continuously, or for a specified number of iterations, to perform a simulation of the simulated system over any desired period of time. (emphasis added).

Having reviewed the cited text of *Yu*, Applicant respectfully submits that the cited text of *Yu* does not teach or suggest "interacting with said control program module". No reference is made by the cited text to any interaction with core **18**, which was identified by the Examiner as a control program module, or any analogous element.

Similarly, Applicant respectfully submits that the cited text of *Yu* does not teach or suggest "instructions on the computer readable medium for interacting with ... said software representation of said plurality of hardware components". The closest that the cited text comes to a teaching or suggestion of "instructions on the computer readable medium for interacting with ... said software representation of said plurality of hardware components" is the cryptic reference to "actions that will be completed in future times in accordance with the simulation models used in the original module definitions used in the simulation" at the end of the fourth quoted paragraph. The cited text may teach and suggest many things, but it does not teach or suggest "instructions on the computer readable medium for providing a testing program for interacting with said control program module and said software representation of said plurality of hardware components." Because the cited text does not teach the recited features for which it is cited, Applicant respectfully submits that the combination of *Yu* and *Lim* does not render unpatentable Applicant's claim 1.

Further, Applicant respectfully submits that the combination of *Yu* and *Lim* does not teach or suggest "instructions on the computer readable medium for, in response to detection of an occurrence of a pre-selected event within said simulated direct access storage device, sending one or more codes from said testing program to said software representation of said plurality of hardware components". The Examiner cites "sending" as being present in "event(2) of FIG. 2". The Examiner then cites Claim 31 as teaching "one or more codes", which are sent from said testing program. The cited text of claim 31 recites:

> 31. A method of simulating the operation of a computing system, comprising providing module definitions defining operations of a computational structure of said computing system, wherein a given segment of a given module definition requests delayed activity at a time identified by reference to a cycle of simulation,
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> translating said given module definition into a first executable object; and
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> producing in response to said given segment, executable code in said first executable object that, during execution, will store a description of said delayed activity with reference to a subsequent cycle of simulation for later retrieval and execution in said subsequent cycle of simulation.

Having reviewed the cited text of *Yu*, Applicant respectfully submits that the *Yu* reference teaches an executable code, which is taught as being distinct and different from a sendable event. The reference does not teach or suggest commingling the two. This distinction is clearly asserted at Column 2, line 26, which asserts that "When an event is delivered to a component modeled by module 16, a child process 22 is formed to execute code in the module." To commingle the sent 'event' of Column 2 with the executed code of Claim 31, which is explained at Column 2, requires an indefensible misreading of the cited content of the reference that would render the *Yu* invention unsuitable for its intended purpose. Applicant respectfully reminds the Examiner that there is no suggestion or motivation to make a modification to the prior art that "would render the prior art invention being modified unsatisfactory for its intended purpose." MPEP 2143.01 (citing *In re Gordon*, 733 F.2d 900, 221 USOQ 1125 (Fed. Cir. 1992). Applicant respectfully submits that the Examiner has not established a *prima facie* case of obviousness, because the Examiner must improperly contort the clear meaning of the reference text to show any teaching or suggestion of the limitations recited in Applicant's Claim 1.

(B) Insufficient motivation is provided to combine the references to obtain Applicant's claimed invention.

With respect to exemplary Claim 1, Applicant respectfully submits that the Examiner's proposed combination of *Yu* and *Lim* does not render obvious Applicant's invention because the proposed combination of *Yu* and *Lim* lacks sufficient evidence of motivation or suggestion to combine the references, which motivation or suggestion is a necessary prerequisite for the proposed combination to render Applicant's invention obvious. M.P.E.P. § 2143. In evaluating motivation or suggestion to combine reference teachings, "a prior art reference must be considered in its entirety, *i.e.*, as a whole" (emphasis in original). M.P.E.P. § 2141.02, citing *W.L. Gore and Associates, Inc. v. Garlock, Inc.*, 721 F.2d 1540, 220 USPQ 303 (Fed. Cir 1983) *cert. denied*, 469 U.S. 851 (1984).

When taken as a whole, *Yu* discloses a simulator *particularly suited* for simulating the hardware/software behavior of embedded systems (*Yu*, abstract). *Yu* describes "a simulator that is appropriate for high complexity systems such as embedded processing systems, such as a digital audio/video decoder" (Col. 3, lines 15-20). Dissimilarly, *Lim* discloses "a flexible and robust planning tool ... for performance evaluation of non-cached and cached DASD systems" (*Lim*, First and second paragraph of introduction). The meaning of 'performance evaluation' is measured in time access time comparison, as is made clear in exhibit 3 on page 1027 of *Lim*. In view of the teachings of the references as taken as a whole, it is apparent that there is no objective suggestion or motivation in the cited references (or generally in the art) that would lead a skilled artisan to combine *the reference teachings* to obtain *the present invention*. It is incumbent upon the Examiner to show, not merely that the combination of the references is advantageous, but that the combination would result in the recited features of Applicant's claim. MPEP 2142, citing *Ex parte Skinner*, 2 USPQ2d 1788 (Bd. Pat. Appl & Inter. 1986). At paragraph 21, the Examiner merely asserts:

> However, Yu does not explicitly teach the simulated device is a simulated direct access storage device.
>
> Lim teaches modeling and simulation of a DASD based on the SIMAN discret-event simulation language [see section 4].

> It would have been obvious to one of ordinary skill in the Data Processing art at the time of the invention was made to apply the behavior simulation for simulating a digital hardware system taught by Yu for simulated direct access storage device as taught by Lim. This modification would have been obvious and a person having ordinary skill in the art would have been motivated to do so because it would enhance the application of the Yu invention.

While the expectation of an advantage, such as general enhancement to *Yu* relied upon by the Examiner, can in some cases provide motivation to combine references, such a motivation is not facially adequate where the combination of references would not result in the present invention. Such an expectation is particularly inadequate as a motivation where, as described above, the combination does not fairly teach or suggest the recited elements for which it is cited.

If a skilled artisan were combine the features of *Yu* with the features of *Lim*, it is not clear whether that skilled artisan would be motivated to derive a system for measuring the access time embedded video decoders, or whether the combination would result in a system for veryifying the electronic design of a DASD. Neither combination is suggested by any teaching in either of the references. What is clear is that it "is impermissible within the framework of Section 103 to pick and choose from any one reference only so much of it as will support a given position, to the exclusion of other parts necessary to the full appreciation of what such reference fairly suggests to one of ordinary skill in the art. " *In re Hedges*, 783 F.2d 1038, 228 USPQ 685, 687 (Fed. Cir. 1992). Absent a specific teaching or suggestion in the references, the Examiner's hindsight choice of a feature set from among the permutations of reference features does not meet his burden to establish a *prima facie* case of obviousness.

The question is whether the prior art, considering its scope and content and the level of ordinary skill, must itself suggest the combination of separate elements into the claimed invention in suit, not just whether it illustrates separate elements....To illustrate this notion, *you cannot claim that the existence of a unicorn should be obvious from taking a trip to the zoo and seeing a horse and a white rhinoceros in adjacent cages.* It takes a spark of inventiveness to look at a horse and a then look at a white rhinoceros and then conceive the idea of a white horse with a horn. Laitram Corporation v. Cambridge Wire Cloth Co., 226 USPQ 289, 293 (D. Md.

1985) (emphasis added). The Examiner's naked assertion of motivation to combine is not sufficient, absent evidence from the references, to establish a *prima facie* case of obviousness.

CONCLUSION

Applicant has diligently responded to the Office Action by showing that the combination of cited references does not teach or suggest the recited features of Applicant's claim. Applicant respectfully submits that Applicant has overcome the Examiner's rejection of the claims under 35 USC §103, and Applicant respectfully requests reconsideration of the rejection and issuance of a Notice of Allowance for all claims now pending.

Applicant further respectfully requests the Examiner contact the undersigned attorney of record at 512.343.6116 if such would further or expedite the prosecution of the present Application.

Respectfully submitted,

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